In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A buffer circuit for a liquid crystal display device comprising: a first transistor further comprising a gate connectable to an input signal, a first electrode coupled to a first power supply, and a second electrode connectable to a second power supply; a second transistor further comprising a gate coupled to the second electrode of the first transistor, a first electrode connectable to the first power supply, and a second electrode connectable to the second power supply; a first capacitor being connectable to the input signal storing a voltage of the input signal when connected to the input signal, and providing a first voltage to the gate of the first transistor when disconnected from the input signal; a second capacitor further comprising a terminal coupled to the second electrode of the first transistor and the gate of the second transistor providing a second voltage at the terminal when the first transistor is turned on; and a third capacitor coupled to the first electrode of the second transistor providing a third voltage when the second transistor is turned on; wherein the second voltage further comprises a first offset including a gate to source voltage of the first transistor, and the third voltage further comprises a second offset including a gate to source voltage of the second transistor.

2. (Original) The circuit of claim 1 further comprising a fourth capacitor including one terminal connectable to the second electrode of the second transistor, and another terminal connectable to the first capacitor.

3. (Original) The circuit of claim 1, the first voltage further comprising the voltage of the input signal.

4. (Original) The circuit of claim 1, the first voltage further comprising a reference voltage.

5. (Original) The circuit of claim 1, the first voltage further comprising the voltage of the input signal and offset voltages including a gate to source voltage each of the first transistor and the second transistor.

6. (Original) The circuit of claim 1, the second voltage further comprising the first voltage and an offset voltage including a gate to source voltage of the first transistor.

7. (Original) The circuit of claim 1, the third voltage being compensated by a threshold voltage each of the first transistor and the second transistor.

8. (Original) The circuit of claim 2, the fourth capacitor providing a fourth voltage when second transistor is turned on.

9. (Original) The circuit of claim 8, the fourth voltage further comprising offset voltages including a gate to source voltage each of the first and second transistors.

10. (Original) A buffer circuit for a liquid crystal display device comprising: a first transistor further comprising a gate connectable to an input signal; a second transistor further comprising a gate coupled to an electrode of the first transistor; a first capacitor being connectable to the input signal and the gate of the first transistor storing a voltage of the input signal when connected to the input signal, and providing the voltage of the input signal to the gate of the first transistor when disconnected from the input signal; a second capacitor coupled to the gate of the second transistor providing a voltage to the gate of the second transistor including a first offset component when the first transistor is turned on; and a third capacitor providing a voltage including a second offset component to neutralize the first offset component when the second transistor is turned on.

11. (Original) The circuit of claim 10, the first offset component further comprising a gate to source voltage of the first transistor.

12. (Original) The circuit of claim 10, the first offset component further comprising a threshold voltage of the first transistor.

13. (Original) The circuit of claim 10, the second offset component further comprising a gate to source voltage of the second transistor.

14. (Original) The circuit of claim 10, the second offset component further comprising a threshold voltage of the second transistor.

15. (Original) A buffer circuit for a liquid crystal display device comprising: a first capacitor being connectable to an input signal storing a reference voltage during a first period, and storing a voltage of the input signal during a second period after the first period; a second capacitor providing a voltage including a first offset during the first period, and providing a voltage including another first offset to neutralize the first offset during the second period; a third capacitor providing a voltage including a second offset during the first period, and providing a voltage including another second offset to neutralize the second offset during the second period; and a fourth capacitor storing the first and second offsets during the first period.

16. (Original) The circuit of claim 15 further comprising a first transistor and a second transistor.

17. (Original) The circuit of claim 16, the first and second offsets further comprising a gate to source voltage of the first transistor and the second transistor, respectively.

18. (Original) The circuit of claim 16, the other first and another second offsets further comprising a gate to source voltage of the first and second transistors, respectively.

19. (Original) The circuit of claim 15, the reference voltage further comprising a zero voltage.

20-33. (Canceled).